ABSTRACT

A new method to form a transistor gate in the manufacture of an integrated circuit device is achieved. The method comprises providing a substrate. A conductor layer is formed overlying the substrate with a dielectric layer therebetween. A masking layer is formed overlying the conductor layer. A resist layer is formed overlying the masking layer. The resist layer is patterned to thereby selectively expose the masking layer. The resist layer exhibits a first spacing between edges of the resist layer. The exposed masking layer is etched through to thereby selectively expose the conductor layer. The etched edges of the masking layer are tapered such that the masking layer exhibits a second spacing between the masking layer edges at the top surface of the conductor layer. The second spacing is less than the first spacing. The exposed conductor layer is etched through to thereby complete a transistor gate.